REMARKS

We have carefully considered the Office Action dated September 10, 2003, in which all the claims are rejected under Section 102 as anticipated by United States Patent 5,796,776 to Lomp et al., and claims 2-6, 8, 10, 12, 14-21 are also rejected under Section 112.

First, we address the Section 112 rejections. We have gone through the claims below in the manner set forth in paragraph 3 of the Office Action and provided the relevant cites to the specification pages:

Claim 2 - "second register" is described in the specification on page 2, lines 14 et seq.; page 4, lines 7 et seq. as, for example, registers $R_1$and R_2 for a degree two polynomial and further registers for higher degree polynomials.

Claim 3 - "selection means" for selecting values of R is described in the specification on page 2, lines 14 et seq.; page 4, line 15 et seq.

Claim 4 - "selection means" for selecting values of, for example, R_1 and R_2, is described in the specification on page 5, at lines 18 et seq.; page 6, lines 1-2.

Claim 5 - "selection means" is discussed above with reference to claim 3, and "means for combining" is described in the specification on page 3 lines 16-21.

Claim 6 - "decrypting system" is described in the specification on page 4, lines 15-23 as a decoder that removes the randomizer sequence from an encyrpted ECC codeword, i.e., decrypts the codeword.

Claim 8 - "means for removing" is described in the specification on page 3, lines 22-24, and "means for detecting" is described in the specification on page 4, lines 24-28.

Claim 10 - "means for providing a key" is described in the specification on page 3, lines 26-28 and again on page 4, lines 12 et seq.

Claim 12 - "means for detecting" and "means for removing" are discussed above with reference to claim 8.

Claim 14 - "means for providing a key" is discussed above with reference to claim 10.

Claim 16 - "plurality of second multipliers" is described in the specification on page 5, line 12 et seq., as, for example, multipliers 102_1 and 102_2 for a degree two polynomial and additional multipliers for higher degree polynomials.

Claim 17 - "encryption means" is described in the specification on page 4, lines 15 et seq.

Claim 18 - "decrypting means" is discussed above with reference to claim 6.

Claim 19 - "selection means" is described in the specification on page 4, lines 15 et seq; page 5 line 1 et seq.

Claim 20 - "encryption means" is discussed above with reference to claim 17.

Claim 21 - "decrypting means" is discussed above with reference to claim 6.

We now discuss the Section 102 rejection. The Lomp system produces spreading codes and despreading codes for use in CDMA modems. The codes are pseudorandom

sequences that repeat, with each repetition corresponding to a code epoch. The spreading code produced by the Lomp system is discussed starting at Column 7, line 60. The code epochs are discussed starting at Column 9, line 53. As is well known, the spreading/despreading codes must repeat so that the encoded signals can be acquired and tracked.

The Lomp system produces the spreading code using a 36-stage linear feedback shift register ("LFSR") that is set up in accordance with an irreducible polynomial h(x) and an associated 128 bit non-linear sequence, as described starting at Column 9, line 4. The LFSR is depicted in Fig. 2 of the Lomp patent and is discussed in more detail along with the related circuitry used to produce the spreading code starting at Column 10, line 22. The Lomp patent does not show, teach or suggest a system and a method of operating a system to produce a non-repeating randomizing sequence.

The Examiner refers to multipliers 704-706, which are included in a "Pilot AVC" circuit that is used to despread a pilot spreading code. See, Column 21, lines 49 et seq. The multipliers 704-706 are components of correlators 701-703. The respective correlators operate in a conventional manner to multiply samples of an input signal by various phases of a pilot spreading code, as part of the pilot code acquisition and tracking operations. The pilot spreading code is generated by pilot code generator 608. See, Column 21, lines 17-20.

The multipliers 704-706 are not included in the system components that generate the pseudorandom spreading code. Accordingly, for this and other reasons, the multipli-

ers 704-706 and/or their operations do not anticipate the multipliers or related method steps of independent claims 1 and 23 and the claims that depend therefrom.

The Examiner also refers to registers 832-835. The registers 832-835 are included in a particular embodiment of the AVC circuit. See, Column 22, lines 17-19 and Column 23, lines 1-19. The registers 832-835 form a shift register that shifts from one register to the next respective message code chips, which are generated by a message code sequence generator 830. See, Column 23, line 6-8. After one or more shifts, the contents of the various registers are multiplied by weighting factors w_1, w_2, and so forth, as part of multipath-related computations. See, Column 23, lines 11-14.

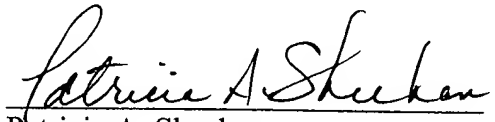
The registers 832-835 are not included in the system components that generate the pseudorandom spreading code. Accordingly, for this and other reasons, the registers 832-835 and/or their operations do not anticipate the registers or related method steps of independent claims 1 and 23 and the claims that depend therefrom.

Further, the Lomp system and/or the method of operating the system do not teach or suggest the current invention. There is no teaching or suggestion in the Lomp patent of a system that produces a non-repeating randomizer sequence, and in particular, of a system that produces the non-repeating randomizer sequence using a multiplier constant that is a selected primitive element of the Galois Field $GF(2^m)$, as set forth in independent claims 1 and 23 and the claims that depend therefrom.

We agree with the Examiner that United States Patent 5,642,377, which is cited as pertinent, does not teach or suggest the current invention.

In light of the above, we request that the Examiner reconsider the rejection of claims 1-36 and issue a Notice of Allowance for all pending claims. Please charge any fee occasioned by this paper to our Deposit Account No. 03-1237.

Respectfully submitted,



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